

to said global word line signal of said global row decoder, wherein  
said local row decoder comprises:

a fifth transistor for transferring said global word line  
signal to said word line in response to (a third signal; )

a sixth transistor for transferring said global word line  
signal to said word line according to (a fourth signal; and

a seventh transistor for transferring a ground voltage to  
said word line in response to a <sup>said third</sup> fifth signal.

REMARKS

Reconsideration and allowance of the above referenced application are respectfully requested. The indication that claims 2-4 and 7-9 would be allowable are appreciatively noted.

The indication that claims 1, 2-4, and 6-9 would be allowable is appreciatively noted. In response, all remaining claims have been amended to now-allowable form.

Claim 1 stands rejected only under 35 U.S.C. 112, second paragraph. In response, claim 1 is amended to include an antecedent basis for "each global word line signal". This should obviate the rejection and render claim 1 allowable.

The drawings stand objected to under Rule 83A as not showing the transistors in claims 7-9. Claims 7-9 have been


canceled to obviate this rejection.

Claim 5 has been amended to include the limitations of claim 6 therein. The limitations have also been amended to obviate the rejections under Section 112.

In view of the above amendments and remarks, therefore, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

Respectfully submitted,

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